Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.200”**



**E**

**B**

**.200”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: E = .020 x .020”**

**B = .010 X .010” min.**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .200” X .200” DATE: 8/4/22**

**MFG: ON SEMI THICKNESS .014” P/N: 2N6857**

**DG 10.1.2**

#### Rev B, 7/19/02